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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,330	10/21/2003	Jin-Hee Kim	5000-1-440	2174
33942	7590	03/20/2008		
CHA & REITER, LLC 210 ROUTE 4 EAST STE 103 PARAMUS, NJ 07652			EXAMINER HAILE, FEBEN	
			ART UNIT 2616	PAPER NUMBER
			MAIL DATE 03/20/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/690,330

Applicant(s)

KIM ET AL.

Examiner

Eben M. Haile

Art Unit

2616

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 12-14 and 17-20 is/are rejected.
- 7) ☒ Claim(s) 6-11 and 15-16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB08)
- Paper No(s)/Mail Date 3/24/2006
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-2 rejected under 35 U.S.C. 103(a) as being unpatentable over Sala et al. (US 2003/0117998), hereinafter referred to as Sala.

Regarding claim 1, Sala discloses providing an Ethernet frame (**Figure 2c; MAC frame**) comprising: a preamble (**element 202; Pre**); a DA (Destination Address) field for indicating a destination address (**element 206; DA**); an SA (Source Address) field for indicating a source address (**element 208; SA**); an L/T (Length/Type) field for indicating a type and length of the Ethernet frame (**element 210; Length/Type**); a data/PAD (Packet Assembly and Disassembly) field for indicating data of the Ethernet frame (**elements 221-220; Data & Pad**); and an FCS (Frame Check Sequence) field which is positioned at an end of the frame and used for detecting an error of the frame when information divided on a frame-by-frame basis is transmitted in data communication (**element 214; FCS**); and reconfiguring the frame with an additional field for indicating a logical link identifier (**element 224; PON tag Control Info**), wherein the reconfigured frame is transferred to the data link layer so that the data link layer uses the LLID field to enable logical MAC emulation (**page 3 paragraph 0045; the tagging**

mechanism allows a MAC control layer to create virtual, i.e. logical, ports to traffic incoming and outgoing optical signals).

Futhermore, Sala teaches a passive optical network consists of an optical line terminal (OLT) that manages communications with a plurality of optical network units (ONUs) **(page 1 paragraph 0006)**, such that a communications path between an OLT and its ONUs is referred to as a PON segment **(page 1 paragraph 0007)**, where a tagging mechanism is implemented to uniquely identify an origin optical node that introduces a frame into the PON segment linking the origin optical node with an upstream optical line terminal **(page 1 paragraph 0009)**. Thus, the equivalence of the instant application's LLID (Logical Link ID) to Sala's PON tag would have been obvious to one of ordinary skill in the art at the time the invention was made. The motivation is to allow a forwarding entity to send a frame back to a port that delivered the frame even if a destination is an end user linked to the incoming PON segment as suggested by Sala on page 1 paragraph 0007.

Regarding claim 2, Sala discloses wherein the Ethernet frame further comprises an E type field for indicating information of an Ether type **(figure 2c element 222; PON tag Type)**.

2. Claims 3-4 and 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (figures 1 and 2), hereinafter referred to as AAPA, in view of Sala et al. (US 2003/0117998), hereinafter referred to as Sala.

Regarding claim 3, AAPA discloses (a) causing a physical layer of the Ethernet passive optical network system to contain LLID (Logical Link ID) information within a

preamble and transfer the preamble containing the LLID information (**figures 1 and 2; an EPON system including a Physical Layer 102 for transferring an Ethernet Frame comprising a preamble including an LLID field**).

However, AAPA fails to explicitly suggest (b) causing an RS (Reconciliation Sublayer) to configure a new Ethernet frame with said preamble and by inserting the LLID information at a predetermined position of the Ethernet frame outside said preamble, and causing the RS to transfer the new Ethernet frame up to a data link layer of the Ethernet passive optical network system; and (c) causing said data link layer to transfer said new Ethernet frame.

Sala teaches (b) causing an RS (Reconciliation Sublayer) (**figure 8 and page 9 paragraph 0019; an ON 106 includes a PHY interface 802, MAC layer 804, and MAC control Layer 806 configured to comply with IEEE standard 802.3**) to configure a new Ethernet frame with said preamble and by inserting the LLID information at a predetermined position of the Ethernet frame outside said preamble, and causing the RS to transfer the new Ethernet frame up to a data link layer of the Ethernet passive optical network system (**page 9 paragraph 0122; where the MAC control 806 adds a PON tag, i.e. LLID information, and then transmits this frame upstream**); and (c) causing said data link layer to transfer said new Ethernet frame (**figure 8 and page 6 paragraph 0082; this PON-tagged frame is then transmitted to a MAC client 808, i.e. OLT**).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method of tagging a MAC frame taught by Sala

into the format of an Ethernet Frame disclosed by AAPA. The motivation for such a modification is an improved Ethernet-based passive optical network for allowing a MAC control layer to create logical ports to traffic incoming and outgoing signals as suggested by Sala on page 2 paragraph 0043.

Regarding claim 4, Sala discloses wherein the new Ethernet frame (**figure 2c; MAC frame**) comprises: a DA (Destination Address) field for indicating a destination address (**element 206; DA**); an SA (Source Address) field for indicating a source address (**element 208; SA**); an LLID field for indicating a logical link identifier (**element 224; PON tag Control info**); an L/T (Length/Type) field for indicating a type and length of the Ethernet frame (**element 210; Length/Type**); a data/PAD (Packet Assembly and Disassembly) field for indicating data of the Ethernet frame (**elements 221-220; Data & Pad**); and an FCS (Frame Check Sequence) field which is positioned at an end of the frame and used for detecting an error of the frame when information divided on a frame-by-frame basis is transmitted in data communication (**element 214; FCS**), wherein the frame in which the LLID field is positioned is transferred to the data link layer so that the data link layer enables logical MAC emulation (**page 3 paragraph 0045; the tagging mechanism allows a MAC control layer to create virtual, i.e. logical, ports to traffic incoming and outgoing optical signals**).

Regarding claim 17, AAPA discloses (a) cause a physical layer of the Ethernet passive optical network system to contain LLID (Logical Link ID) information within a preamble and transfer the preamble containing the LLID information (**figures 1 and 2**;

an EPON system including a Physical Layer 102 for transferring an Ethernet Frame comprising a preamble including an LLID field).

However, AAPA fails to explicitly suggest (b) cause an RS (Reconciliation Sublayer) to configure a new Ethernet frame with said preamble and by inserting the LLID information at a predetermined position of the Ethernet frame outside said preamble, and causing the RS to transfer the new Ethernet frame up to a data link layer of the Ethernet passive optical network system; and (c) cause said data link layer to transfer said new Ethernet frame.

Sala teaches instructions which, when executed by a processor (**page 10 paragraph 0139; computer programs, when executed, enable a processor to implement the process of the present invention**) cause (b) causing an RS (Reconciliation Sublayer) (**figure 8 and page 9 paragraph 0119; ON 106 includes a PHY interface 802, MAC layer 804, and MAC control Layer 806 configured to comply with IEEE standard 802.3**) to configure a new Ethernet frame with said preamble and by inserting the LLID information at a predetermined position of the Ethernet frame outside said preamble, and causing the RS to transfer the new Ethernet frame up to a data link layer of the Ethernet passive optical network system (**page 9 paragraph 0122; where the MAC control 806 adds a PON tag, i.e. LLID information, and then transmits this frame upstream**); and (c) causing said data link layer to transfer said new Ethernet frame (**figure 8 and page 6 paragraph 0082; this PON-tagged frame is then transmitted to a MAC client 808, i.e. OLT**).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method of tagging a MAC frame taught by Sala into the format of an Ethernet Frame disclosed by AAPA. The motivation for such a modification is an improved Ethernet-based passive optical network for allowing a MAC control layer to create logical ports to traffic incoming and outgoing signals as suggested by Sala on page 2 paragraph 0043.

3. Claims 12-14 and 18-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Sala et al. (US 2003/0117998), hereinafter referred to as Sala, in view of Applicants Admitted Prior Art (figures 1 and 2), hereinafter referred to as AAPA.

Regarding claim 12, Sala discloses (a) causing a data link layer of the Ethernet passive optical network system to transfer an Ethernet frame containing LLID (Logical Link ID) information (**figure 9 and page 9 paragraph 0124; an OLT 102 transfers a PON-tagged frame to a PHY interface 902, MAC layer 904, and MAC control Layer 906 configured to comply with IEEE standard 802.3**); (b) causing an RS (Reconciliation Sublayer) (**figure 9 and paragraph 0124; OLT 102 includes a PHY interface 902, MAC layer 904, and MAC control Layer 906 configured to comply with IEEE standard 802.3**) to extract the LLID information contained in the Ethernet frame and configure a standard-based Ethernet frame by inserting the LLID information in a preamble, and causing the RS to transfer the standard-based Ethernet frame to a lower physical layer of the Ethernet passive optical network system (**page 10**

paragraph 0130; the MAC control Layer 906 removes the PON tag, i.e. LLID information, and then transmits this frame downstream).

Sala fails to explicitly suggest (c) causing the physical layer to transfer the preamble containing the LLID information.

AAPA teaches (c) causing the physical layer to transfer the preamble containing the LLID information **(figures 1 and 2; an EPON system including a Physical Layer 102 for transferring an Ethernet Frame comprising a preamble including an LLID field).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method of transmitting an Ethernet Frame disclosed by AAPA into the method of tagging a MAC frame taught by Sala into. The motivation for such a modification is so that the emulation can be performed as if a single physical MAC layer corresponds to a plurality of logical MAC layers as suggested by AAPA on page 2 lines 15-17.

Regarding claim 13, Sala discloses wherein the Ethernet Frame containing the LLID information **(figure 2c; MAC frame)** comprises: a DA (Destination Address) field for indicating a destination address **(element 206; DA)**; an SA (Source Address) field for indicating a source address **(element 208; SA)**; an LLID field for indicating a logical link identifier **(element 224; PON tag Control Info)**; an L/T (Length/Type) field for indicating the Ethernet frame's length and type **(element 210; Length/Type)**; a data/PAD (Packet Assembly and Disassembly) field for indicating data of the Ethernet frame **(elements 221-220; Data & Pad)**; and an FCS (Frame Check Sequence) field

which is positioned at an end of the frame and used for detecting an error of the frame when information divided on a frame-by-frame basis is transmitted in data communication **(element 214; FCS)**, wherein said frame containing LLID information is transferred to the data link layer so that the data link layer uses the LLID field to enable logical MAC emulation **(page 3 paragraph 0045; the tagging mechanism allows a MAC control layer to create virtual, i.e. logical, ports to traffic incoming and outgoing optical signals)**.

Regarding claim 14, Sala discloses wherein said Ethernet frame containing LLID information further comprises an E type field for indicating information of an Ether type **(element 222; PON tag Type)**.

Regarding claim 18, Sala discloses instructions which, when executed by a processor **(page 10 paragraph 0139; computer programs, when executed, enable a processor to implement the process of the present invention)** cause (a) cause a data link layer of the Ethernet passive optical network system to transfer an Ethernet frame containing LLID (Logical Link ID) information **(figure 9 and page 9 paragraph 0124; an OLT 102 transfers a PON-tagged frame to a PHY interface 902, MAC layer 904, and MAC control Layer 906 configured to comply with IEEE standard 802.3)**; (b) cause an RS (Reconciliation Sublayer) **(figure 9 and paragraph 0124; OLT 102 includes a PHY interface 902, MAC layer 904, and MAC control Layer 906 configured to comply with IEEE standard 802.3)** to extract the LLID information contained in the Ethernet frame and configure a standard-based Ethernet frame by inserting the LLID information in a preamble, and causing the RS to transfer the

standard-based Ethernet frame to a lower physical layer of the Ethernet passive optical network system (**page 10 paragraph 0130; the MAC control Layer 906 removes the PON tag, i.e. LLID information, and then transmits this frame downstream).**

Sala fails to explicitly suggest (c) cause the physical layer to transfer the preamble containing the LLID information.

AAPA teaches (c) cause the physical layer to transfer the preamble containing the LLID information (**figures 1 and 2; an EPON system including a Physical Layer 102 for transferring an Ethernet Frame comprising a preamble including an LLID field).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method of transmitting an Ethernet Frame disclosed by AAPA into the method of tagging a MAC frame taught by Sala into. The motivation for such a modification is so that the emulation can be performed as if a single physical MAC layer corresponds to a plurality of logical MAC layers as suggested by AAPA on page 2 lines 15-17.

Regarding claim 19, Sala discloses wherein the Ethernet Frame containing the LLID information (**figure 2c; MAC frame**) comprises: a DA (Destination Address) field for indicating a destination address (**element 206; DA**); an SA (Source Address) field for indicating a source address (**element 208; SA**); an LLID field for indicating a logical link identifier (**element 224; PON tag Control Info**); an L/T (Length/Type) field for indicating the Ethernet frame's length and type (**element 210; Length/Type**); a data/PAD (Packet Assembly and Disassembly) field for indicating data of the Ethernet

frame (**elements 221-220; Data & Pad**); and an FCS (Frame Check Sequence) field which is positioned at an end of the frame and used for detecting an error of the frame when information divided on a frame-by-frame basis is transmitted in data communication (**element 214; FCS**), wherein said frame containing LLID information is transferred to the data link layer so that the data link layer uses the LLID field to enable logical MAC emulation (**page 3 paragraph 0045; the tagging mechanism allows a MAC control layer to create virtual, i.e. logical, ports to traffic incoming and outgoing optical signals**).

Regarding claim 20. Sala discloses wherein said Ethernet frame containing LLID information further comprises an E type field for indicating information of an Ether type (**element 222; PON tag Type**).

Allowable Subject Matter

4. Claims 6-11 and 15-16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Feben M. Haile whose telephone number is (571) 272-3072. The examiner can normally be reached on 10:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung S. Moe can be reached on (571) 272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Feben M Haile/
Examiner, Art Unit 2616

/Aung S. Moe/

Supervisory Patent Examiner, Art Unit 2616

